

## PATENT ABSTRACTS OF JAPAN

(11)Publication number : 01-169492  
 (43)Date of publication of application : 04.07.1989

(51)Int. CI. G09G 1/02  
 G06F 3/153  
 G09G 1/00  
 G09G 1/00  
 G09G 1/00  
 H04N 1/387

(21)Application number : 63-132540 (71)Applicant : COMMODORE ELECTRON LTD  
 (22)Date of filing : 30.05.1988 (72)Inventor : DAVIS HEDLEY C

## (30)Priority

Priority number : 87 55608 Priority date : 29.05.1987 Priority country : US

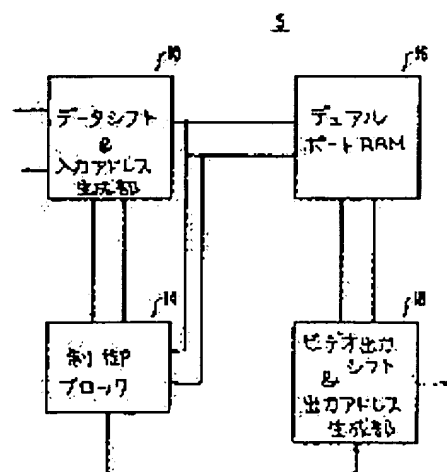
## (54) HIGH-RESOLUTION VIDEO OUTPUT FRAME GENERATION SYSTEM

## (57)Abstract:

PURPOSE: To improve resolution at low cost by storing video input data at a 1st clock speed, connecting a selected line and generating one line, and outputting a line which is generated with a 2nd faster clock.

CONSTITUTION: Video input data are inputted by a data shift and input address conversion part 10 and put in plural frames at the 1st clock speed. One of the frames is selected and the line corresponding to the frame is connected to form one line. Further, the line is outputted by a video output shift and address conversion part 18 with the 2nd existent clock faster than the 1st clock. Thus, a computer device video output channel which is designed for low resolution is used to output video frame data of high horizontal and high vertical resolution to a display device which has no frame buffer.

BEST AVAILABLE COPY



## LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision  
of rejection]

[Date of requesting appeal against examiner's  
decision of rejection]

[Date of extinction of right]

Copyright (C); 1998, 2003 Japan Patent Office